



## Regulations Concerning the Setting up of Installations

Apart from the basic "Regulations for the Setting up of Power Installations" DIN VDE\* 0100 and for "The Rating of Creepage Distances and Clearances" DIN VDE 0110 Part 1 and Part 2 the regulations "The Equipment of Power Installations with Electrical Components" DIN VDE 0160 in conjunction with DIN VDE 0660 Part 500 have to be taken into due consideration.

Further attention has to be paid to DIN VDE 0113 Part 1 and Part 200 in case of the control of working and processing machines. If operating elements are to be mounted near parts with dangerous contact voltage DIN VDE 0106 Part 100 is additionally relevant.

If the protection against direct contact according to DIN VDE 0160 is required, this has to be ensured by the user (e.g. by incorporating the elements in a switch-gear cabinet). The devices are designed for pollution severity 2 in accordance with DIN VDE 0110 Part 1. If higher pollution is expected, the devices must be installed in appropriate housings.

The user has to guarantee that the devices and the components belonging to them are mounted following these regulations. For operating the machines and installations, other national and international relevant regulations, concerning prevention of accidents and using technical working means, also have to be met.

The Advant Controller 31 (AC31) standard devices are designed according to IEC 1131 Part 2. Meeting this regulation, they are classified in overvoltage category II which is in conformance with DIN VDE 0110 Part 2.

For the direct connection of AC31 devices, which are powered with or coupled to AC line voltages of overvoltage category III, appropriate protection measures corresponding to overvoltage category II according to IEC-Report 664/1980 and DIN VDE 0110 Part 1 are to install.

Equivalent standards:

DIN VDE 0110 Part 1 corresponds to IEC 664  
DIN VDE 0113 Part 1 corresponds to EN 60204 Part 1  
DIN VDE 0660 Part 500 corresponds to EN 60439-1  
corresponds to IEC 439-1

The safety-related checklist has to be fulfilled. System operation is only allowed when the switch cabinet is closed.

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\* VDE stands for "Association of German Electrical Engineers".

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# 1 Safety-related checklist, general

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The safety-related checklist predefines the frame for the management of a project using a safety-related PLC.

## General sequence:

- Checking of the restrictions, according to the rules of the Certification Report, see volume 2 chapter 1.1 "Certification Report"
- Concept phase by the user
- Presentation of the concept to the experts' authority (TÜV, professional partnership, insurance company, etc.)
- Fixing the safety conditions by the experts' authority
- Planning the software by the user
- Presentation of the planning documents to the experts' authority
- Pre-check by the experts' authority
- Completing the planning by the user
- Realization of software and hardware by the user
- Presentation of the realization documents to the experts' authority
- Completing the realization by the user
- Safety-technical judgement including inspection at the site and acceptance

The sequence may vary as to the order or number of iterations concerning presentation and inspection.

## 1.1 Concept phase

- Verbal description of the problem and requirements including extent, marginal conditions and special items
- Rough functional flow chart

## 1.2 Software planning

- Problem documentation and structuring, data flow, acquisition and description of all states, summary in form of a detailed flow chart
- Division into safety-related and non-safety-related part
- Adjust "Global flag setting" in the menu for all safety modules (see volume 4, chapter 4.4 data structure, page 1-2)
- Determination of the operating states
- Definition of the system reactions in case of internal and external errors
- Determining the required signals and splitting up according to:
  - safety-related input signals
  - safety-related output signals
  - safety-related analog input signals
  - non-safety-related input signals
  - non-safety-related output signals
  - non-safety-related analog input signals
  - non-safety-related analog output signals
- Definition of:
  - reserves for safety-related input signals
  - reserves for safety-related output signals
  - reserves for safety-related analog input signals
  - reserves for non-safety-related input signals
  - reserves for non-safety-related output signals
  - reserves for non-safety-related analog input signals
  - reserves for non-safety-related analog output signals
- Definition of external interfaces (e.g. connections to host computers, operating terminals, network)
- Backup of data which are to be read indirectly via S\_IDL

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\*) Check the predefined default values whether they are sufficient for this application.

- Definition of the required
  - times
  - counters
  - work flags for safety-related input modules \*)
  - work flags for safety-related output modules \*)
  - work flags for safety-related analog input modules \*)
- MMC concept, definition of signals
  - in case of errors
  - Concept for variable distribution (data range editor) \*)
  - module-related definition of local flags \*)
  - module-related definition of global flags \*)
  - Definition of default values for safe state (at certain safety-related CEs, values for the PLC can be predefined)
  - Which error must trigger a system standstill?
  - Which error can be tolerated?
  - Which errors trigger a partial shutdown of the system (e.g. load-reducing measures)?
  - Development environment for the Advant Controller 31-S (the latest version of the 907 PC 339 must always be available; is the existing PC suited for the software, see hardware pre-conditions)?
- Documentation complete?
  - Software
  - Variable list
  - Program parts
  - System behaviour, necessary for the realization

### 1.3 Hardware planning

- Hardware components according to signal definitions and determining the I/O points observing the assignment restrictions
  - Number of safety-related input modules
  - Number of safety-related output modules
  - Number of safety-related analog input modules
  - Number of non-safety-related input modules
  - Number of non-safety-related output modules
  - Number of non-safety-related analog input modules
  - Number of non-safety-related analog output modules
- Determining the current consumption for selecting the power supply
- Specifications for the mains supply observed? (see volume 3, section 3.4)
- Wiring concept
- EMC concept
- Lightning protection concept
- Hardware documentation
  - Module configuration
  - Wiring

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\*) Check the predefined default values whether they are sufficient for this application.

## 1.4 Software realization

- Latest software 907 PC 339 used?
- "Global flag setting" for all safety modules adjusted ? (see volume 4, chapter 4.4 datastructure, page 1-2)
- Safety-relevant signals defined?
- Problem documentation and structuring, data flow
- Division into safety-related and non-safety-related part
- Concept for variable split up
- Default values for safe state
- Indirect reading (S\_IDL) of safety-related data only?
- Program generation exclusively in FBD
- Maximum cycle time correctly set? (see volume 3, chapter 3.1.2)
- Error reaction planned?
- System reaction correctly set?
- Check global flags in data range editor for overlapping using function key in overall data range editor
- Time delay of program start HW/SW
- FBD translated completely and error-free in all modules?
- Generate control code (menu item "Config.PLC", "Translate")
- Send program (program storage in RAM)
- Save program in Flash-EEPROM via operating command "SP". If a SmartMediaCard is inserted, the program is also stored in the SMC.
- Compare program (program in PC with controller)
- Test software in RAM
- Determine system reaction time from hardware-related times and PLC cycle time
- Software documentation via FBD listing and print information in modularization editor
- Flag documentation via data range editor listing
- Time documentation via variable editor
- System behaviour documentation
- Difference listing documentation
- Copy IL (instruction list) in file (for comparison operation)
- Archiving of project files and libraries
- Documentation, current version 907 PC 339

## 1.5 Hardware realization

- Hardware components / safety-related modules
  - Address setting correct
  - Assignment of signal inputs complete
  - Assignment of signal outputs complete
  - Assignment of unused inputs complete
  - All terminal blocks plugged
- Non-safety-related modules
  - Bus termination resistor present
  - Address setting of AC31 modules correct
- Power supply
- Wiring/EMC concept observed
- Wiring
  - Module supply
  - Shield CS31-bus line connected to PLC (07 KT 94-S)
  - Shield CS31-bus line connected to safety-related modules
  - Shield CS31-bus line connected to non-safety-related modules
  - Shield of analog signals connected
  - Earth connection of PLC (07 KT 94-S) assigned
  - Earth connection of safety-related modules assigned
  - Earth connection of power supplies for the PLC assigned
  - Earth connection of power supplies for process supply assigned
  - Required conductor cross sections used
  - Required signal lines used
  - Required CS31-bus lines used
  - Correct earthing of shields
- Lightning protection concept defined and realized
- If the 07 KT 94-S basic unit is used, it must be made sure, that the cabinet temperature does not fall below 0°C.

## 1.6 Safety-related examination

- Init part complete, i.e. are S\_App-S and S\_App-N present?
- Have all times and safety-related step chains been initialized?
- No overlapping of safety variables (global flags and labels)?
- No overlapping of times?
- Only safety-related CEs in safety-related part (S\_App-S) used?
- Indirect reading of backed-up data only?
- Error reaction planned?
- Error signalization planned?
- Error reaction time <200 msec?
- Archiving
  - Documentation
  - Software
  - EPROM
- Program comparison between PLC and programming system carried out? (main menu, PLC communic. 1, Compare overall program)
- Program saved from RAM memory to Flash-EPROM?
- With the 07 KT 94-S basic unit, the CE S\_TSYNC is monitored by the operating system in the background. Programming by the user is not necessary
- Starts the PLC only if all planned modules are logged on to the bus? The number of modules at the bus must be entered in constant KW00,09. Example: KW00,09 = +7
- Measuring of the error reaction times and switch-off times if necessary.
- Is a monitoring of UP prescribed? Is it active?
- Are the ARCNET and networking interface used for non safety-related data/signals only?

## 1.7 Commissioning and test

- Hardware
  - Completeness of all modules
  - Address setting of bus participants
  - Check of wiring
    - Earthing
    - Process power supply
  - Bus
  - Signals
  - Error signalization
  - Error reaction
- Software
  - System reaction modified
  - Address setting of the CEs
  - Execute all program parts once
  - Check functioning of program parts
  - Check functioning of overall system
  - Check system reaction time
- Error tests
  - Sensor cut wire
  - Bus interruption
  - Safety shut-down of the output modules

## 1.8 Documentation

- Version of the programming SW in the user program
- Archiving
- Program module list
- Cross reference list
- FBD list
- Variable list
- Data ranges
- System configuration
- Difference listing
- Wiring
- Module list

## 1.9 Safety regulations

- Have all standard regulations for the respective application be observed?
- Have all dependencies been considered?
- Have all possible failures be considered?
- Protective measures against external influences or unauthorized accesses
  - RUN/STOP-switch in position RUN and control cabinet locked?
  - Interface to AC31-S not assigned?
  - Forces locked?
  - Online program changes locked?
- Have all conditions by the manufacturer of the overall system been kept?

## 1.10 Program modifications

- Precondition: the S program in the Flash was tested.
- Have program changes been made exclusively in the FBD of the non-safety-related program module?
- Has the FBD been translated completely error-free?
- Has the control code been created?
- Was the software test in the RAM error-free?
- Was the program saved in Flash-EEPROM?
- Code comparison error-free?
- Copy IL in file
- Start comparison program indicating and proving the changes made
- Software documentation via FBD listing and print information in modularization editor
- Archiving of project files and libraries



## 2 Additional safety-related checklist for road traffic signal systems

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The additional safety-related checklist predefines the frame for the management of a project using a safety-related PLC in conjunction with road traffic signal systems.

Road traffic signal systems may only be set up by skilled persons with professional training, who possess pertinent knowledge and experience in the fields of telecommunication, electrical power installation and road traffic systems. They must be able to use relevant standards and regulations and to assess possible danger in connection with their tasks and concerning the traffic users.

With road traffic signal systems, the following items have to be fulfilled in addition to the general safety-related check list (chapter 1).

### 2.1 Concept phase

- Setting up the signal position diagram, the signal time diagram and the security table
- Definition of the operating modes

### 2.2 Software planning

- Classifying into indispensable, dispensable by condition and dispensable security measures
- Definition of the security measures of signals
  - against lost signals
  - against unwanted appearing signals (signal green against hostile signal green)
  - changes of signal times
- Definition of the safety-related signal times
- Definition of the signals of a signal group
- Evaluation of signal position diagram, signal time diagram and security table of a traffic junction
- Definition of an auxiliary operation mode (including auxiliary signal diagram)
- Definition of event signalling units for failing signals
- Definition of the power-on behaviour (first power-on or power-on after error remedy)

### 2.3 Hardware planning

- Definition of equipment according to DIN VDE 0832
- Definition of set-up requirements according to DIN VDE 0832

### 2.4 Software realization

- Carrying out of security measures against traffic-endangering signal statuses with the aid of comparative circuits and interlocking circuits (if necessary)
  - against failing signals (signal red defective)
  - against unwanted appearing signals (signal green against hostile signal green)
  - changes of signal times
- Implementation of the safety-related signal times
- Implementation of the signals of one signal group
- Evaluation of signal position diagram, signal time diagram and security table of a traffic junction
- Implementation of an auxiliary operation mode (including auxiliary signal diagram)
- Implementation of event signalling units for failing signals
  - for single signal transmitter
  - with OR combination for lamp failure of signal transmitters connected in parallel
  - with AND combination for lamp failure of signal transmitters connected in parallel
  - for signal transmitters connected in parallel
  - for optical devices configured twice or for double-optical devices
  - for two-filament lamps with filament switch-over
- Definition of the individual switch-over behaviour (first power-on or power-on after error remedy)

## 2.5 Hardware realization

- Planning of equipment according to DIN VDE 0832
- Installation according to the set-up requirements of DIN VDE 0832
  - Connection to the power supply
  - Electrical equipment under lock and key
  - Main switch in the switch and control unit
  - Operating mode selector switch
  - Dimensioning and protection of wires and cables
  - Installation of wires and cables
- Definition of the power-on behaviour (first power-on or power-on after error remedy)
- Has the auxiliary mode been planned (including auxiliary signal diagram)?
- If the 07 KT 94-S basic unit is used, it must be made sure, that the cabinet temperature does not fall below 0°C.

## 2.6 Safety-related examination

- Are the security measures against traffic-endangering signal statuses performed correctly? (with the aid of comparative circuits and interlocking circuits, if necessary).
  - against failing signals (signal red defective)
  - against unwanted appearing signals (signal green against hostile signal green)
  - changes of signal times
- Has the effectiveness of the comparative circuits been checked?
- Come the comparative circuits into effect after < 300 ms, if a traffic endangering signal status occurs?
- Are the safety-related signal times observed?
- Are the signals of a signal group implemented and equal according to the specifications?
- Do the signal position diagram, the signal time diagram and the security table of a traffic junction match to one other?

- Are event signalling units implemented for failing signals?
  - for single signal transmitter
  - with OR combination for lamp failure of signal transmitters connected in parallel
  - with AND combination for lamp failure of signal transmitters connected in parallel
  - for signal transmitters connected in parallel
  - for optical devices configured twice or for double-optical devices
  - for two-filament lamps with filament switch-over

## 2.7 Commissioning and test

- Has a function check of the signal environment been performed?
- Has a function check of the signal security been performed?
- Have the security measures against traffic endangering signal statuses been carried out?
  - against failing signals (signal red defective)
  - against unwanted appearing signals (signal green against hostile signal green)
  - changes of signal times
- Have the tests of the road traffic signal system been carried out after commissioning according to DIN VDE 0832?

## 2.8 Documentation

- Technical documentation according to DIN VDE 0832, chapter 10.9

## 3 Diagnosis and troubleshooting

For diagnosis and troubleshooting the existing diagnosis system of the Advant Controller was used and extended with additional messages. All error messages, which represent a violation of the safety-related functions, release an error of the error class FK2 on the central unit. If a FK2 is detected, the program processing stops, the safety-related outputs are carried into safe state (outputs are switched off) and the LED FK2 on the central unit is activated. The error handshaking after fault

clearance is done by switching-off/on the 24 V supply voltage of the overall system.

### 3.1 Error identification for FK2 errors

The following tables contain a more detailed error description. These messages are displayed in terminal operation or in diagnosis flags.

Error class	Error description	Error identifier in MW 254,08		Detailed info 1 in MW 254,09	Detailed info 2 in MW 254,10	Detailed info 3 in MW 254,11	Further detailed info in MW 254,12 : MW 254,15
		Dec	Hex	YYYY	ZZZZ *)		
FK2	S_EB: Input does not comply with binary safety-related data format	510 <sub>D</sub>	01FE <sub>H</sub>	Address	Additional information		
	S_AB: Output does not comply with binary safety-related data format	511 <sub>D</sub>	01FF <sub>H</sub>	Address	Additional information		
	S_EA: Input does not comply with analog safety-related data format	515 <sub>D</sub>	0203 <sub>H</sub>	Address	Additional information		
	S_AA: Output does not comply with analog safety-related data format	516 <sub>D</sub>	0204 <sub>H</sub>	Address	Additional information		
	EB: Input does not comply with binary data format	520 <sub>D</sub>	0208 <sub>H</sub>	Address	Additional information		
	AB: Output does not comply with binary data format	521 <sub>D</sub>	0209 <sub>H</sub>	Address	Additional information		
	B_ADR: assigned binary input has wrong address	522 <sub>D</sub>	020A <sub>H</sub>	Address	Additional information		
	EA: Input does not comply with analog data format	525 <sub>D</sub>	020D <sub>H</sub>	Address	Additional information		
	AA: Output does not comply with analog data format	526 <sub>D</sub>	020E <sub>H</sub>	Address	Additional information		
	A_ADR: assigned analog input has wrong address	527 <sub>D</sub>	020F <sub>H</sub>	Address	Additional information		
	S_INT: internal processing error	530 <sub>D</sub>	0212 <sub>H</sub>	Address	Additional information		
	SQRT_NEG: negative input E1 at CE SQRT	540 <sub>D</sub>	021C <sub>H</sub>	Address	Additional information		
	TIMER: error timer call (no free timer is available)	541 <sub>D</sub>	021D <sub>H</sub>	Address	Additional information		

\*) see the following pages

Error class	Error description	Error identifier in MW 254,08		Detailed info 1 in MW 254,09	Detailed info 2 in MW 254,10	Detailed info 3 in MW 254,11	Further detailed info in MW 254,12 : MW 254,15
		Dec	Hex	YYYY	ZZZZ *)		
<b>FK2</b>	ABORT: program abort by CE S_ABO correctly released	542 <sub>D</sub>	021E <sub>H</sub>	Address	Additional information		
	ADR<>MODN: input ADR and MODN do not match	543 <sub>D</sub>	021F <sub>H</sub>	Address	Additional information		
	CRC: internal error while calling CRC-calculation	544 <sub>D</sub>	0220 <sub>H</sub>	Address	Additional information		
	COUNT: loop counter (Iteration) overflow - internal error	545 <sub>D</sub>	0221 <sub>H</sub>	Address	Additional information		
	ANZ: max. number of nodes exceeded	546 <sub>D</sub>	0222 <sub>H</sub>	Address	Additional information		
	TSYNC_TOD: TSYNC-error - clock doesn't run	547 <sub>D</sub>	0223 <sub>H</sub>	Address	Additional information		
	TSYNC_KL: TSYNC-error - clock is running too slow	548 <sub>D</sub>	0224 <sub>H</sub>	Address	Additional information		
	TSYNC_GR: TSYNC-error - clock is running too fast	549 <sub>D</sub>	0225 <sub>H</sub>	Address	Additional information		

Error class	Error description	Error identifier in MW 254,08		Detailed info 1 in MW 254,09	Detailed info 2 in MW 254,10	Detailed info 3 in MW 254,11	Further detailed info in MW 254,12 : MW 254,15
		Dec	Hex	YYYY	ZZZZ		
<b>FK2</b>	Program run number	550 <sub>D</sub>	0226 <sub>H</sub>	Address			
	EPROM checksum	551 <sub>D</sub>	0227 <sub>H</sub>	Address			
	Segment pointer	552 <sub>D</sub>	0228 <sub>H</sub>	Address			
	Check operand memory	553 <sub>D</sub>	0229 <sub>H</sub>	Address			
	Check RAM 1	554 <sub>D</sub>	022A <sub>H</sub>	Address			
	Check ARCNET memory	555 <sub>D</sub>	022B <sub>H</sub>	Address			
	Check constant memory	556 <sub>D</sub>	022C <sub>H</sub>	Address			
	CRC16 from AWP	557 <sub>D</sub>	022D <sub>H</sub>	Address			
	CRC16 from turbo memory	558 <sub>D</sub>	022E <sub>H</sub>	Address			
	CPU check	559 <sub>D</sub>	022F <sub>H</sub>	Address			

\*) see the following pages

For more detailed error detection refer to the following table.

### 3.2 List of additional information related to CE groups 1...6

FK2 number	Error description
510	Input does not comply with binary safety-related data format
511	Output does not comply with binary safety-related data format
515	Input does not comply with analog safety-related data format
516	Output does not comply with analog safety-related data format
520	Input does not comply with binary data format
521	Output does not comply with binary data format
523	wrong I/O connection at ADR channel ; S_VEs S_LEB, S_LEA, S_LAB, S_SAB
522	assigned binary input has wrong address
525	Input does not comply with analog data format
526	Output does not comply with analog data format
527	assigned analog input has wrong address
530	internal processing error
540	negative input E1 at CE SQRT
541	error while timer call (no free timer is available)
542	error by CE S_ABO correctly released
543	input ADR and MODN do not match
544	internal error while calling the CRC-calculation
545	loop counter (iteration) overflow
546	max. number of nodes exceeded
547	TSYNC-error - clock doesn't run
548	TSYNC-error - clock is running too slow
549	TSYNC-error - clock is running too fast
550	Error program run number; program run number of "PA" is unequal the calculated program run number.
551	Entered EPROM-checksum is unequal the calculated checksum.
552	Segment pointer for calculation of the checksum is not 0, E000 <sub>H</sub> or F000 <sub>H</sub> , RAM error.
553	Write-/read error while operand memory check detected.
554	Write-/read error while RAM check (organization part of operating system EBS).
555	Write-/read error in ARCNET memory detected.
556	Compare error while comparing constant memory with constant range in operand memory.
557	Compare error while CRC16 check of the user memory detected.
558	Compare error while CRC16 check of the turbo memory detected.
559	Error while CPU check, CPU doesn't work correct or the registers are not o.k.
560	Error while transferring the background checks. ( $0 \leq \text{counter} \leq 8$ ).
570	RAM error; a difference was detected while saving and subsequently playing back the segment and offset address.

CE Name	FK2: 510	FK2: 511	FK2: 515	FK2: 516	FK2: 520	FK2: 521	FK2: 522	FK2: 525	FK2: 526	FK2: 527	FK2: 530	FK2: 540	FK2: 541	FK2: 542	FK2: 543	FK2: 544	FK2: 545	FK2: 546	FK2: 547	FK2: 548	FK2: 549	Additional information	Direct ERR output	
<b>Group 1</b>																								
S_LEB	X	X					X				X		X		X	X							50 <sub>H</sub> : Addr. < E0,0 60 <sub>H</sub> : Addr. > E62,0 70 <sub>H</sub> : Chan. no. <> 0 80 <sub>H</sub> : Addr. <> Mod. no. 90 <sub>H</sub> : ERR CRC calcul. 100 <sub>H</sub> : No free timer 11x <sub>H</sub> : Input Dx not S_EB (x = input no.) 120 <sub>H</sub> : ERR writing output 130 <sub>H</sub> : ERR writing memory	10 <sub>D</sub> : CRC8 comparison error 20 <sub>D</sub> : Module number comparison error 30 <sub>D</sub> : Running number error
S_LEA			X	X						X	X		X		X	X							50 <sub>H</sub> : Addr. < EW0,0 60 <sub>H</sub> : Addr. > EW6,0 70 <sub>H</sub> : Chan. no. <> 0 80 <sub>H</sub> : Addr. <> Mod. no. 90 <sub>H</sub> : ERR CRC calcul. 100 <sub>H</sub> : No free timer 11x <sub>H</sub> : Inputs Dx/DxN not S_EA (x = input no.) 120 <sub>H</sub> : ERR writing output 130 <sub>H</sub> : ERR writing memory	10 <sub>D</sub> : CRC8 comparison error 20 <sub>D</sub> : Module number comparison error 30 <sub>D</sub> : Running number error
S_LAB		X					X				X		X		X	X							50 <sub>H</sub> : Addr. < A0,0 60 <sub>H</sub> : Addr. > A62,0 70 <sub>H</sub> : Chan. no. <> 0 80 <sub>H</sub> : Addr. <> Mod. no. 90 <sub>H</sub> : ERR CRC calcul. 100 <sub>H</sub> : No free timer 120 <sub>H</sub> : ERR writing output 130 <sub>H</sub> : ERR writing memory	10 <sub>D</sub> : CRC8 comparison error 20 <sub>D</sub> : Module number comparison error 30 <sub>D</sub> : Running number error

CE Name	FK2: 510	FK2: 511	FK2: 515	FK2: 516	FK2: 520	FK2: 521	FK2: 522	FK2: 525	FK2: 526	FK2: 527	FK2: 530	FK2: 540	FK2: 541	FK2: 542	FK2: 543	FK2: 544	FK2: 545	FK2: 546	FK2: 547	FK2: 548	FK2: 549	Additional information	Direct ERR output	
S_SAB	X	X					X				X				X	X							10 <sub>H</sub> : Input GA not S_EB 2x <sub>H</sub> : Input Dx not S_EB (x = input no.) 50 <sub>H</sub> : Addr. < A0,0 60 <sub>H</sub> : Addr. > A62,0 70 <sub>H</sub> : Chan. no. <> 0 80 <sub>H</sub> : Addr. <> Mod. no. 90 <sub>H</sub> : ERR CRC calcul. 120 <sub>H</sub> : ERR writing output 130 <sub>H</sub> : ERR writing memory	10 <sub>D</sub> : CRC8 comparison error 20 <sub>D</sub> : Module number comparsion error 30 <sub>D</sub> : Running number error

CE Name	FK2: 510	FK2: 511	FK2: 515	FK2: 516	FK2: 520	FK2: 521	FK2: 522	FK2: 525	FK2: 526	FK2: 527	FK2: 530	FK2: 540	FK2: 541	FK2: 542	FK2: 543	FK2: 544	FK2: 545	FK2: 546	FK2: 547	FK2: 548	FK2: 549	Additional information	Direct ERR output
<b>Group 2</b>																							
S_IW			X																				
S_IW-			X																				
S_=W				X																			
S_=W-				X																			
S_+			X								X												
S_-			X								X												
S_*			X								X												
S_:			X								X												
S_BEG			X	X							X												
S_IDL	X		X								X												
S_AWT	X		X								X												
S_SQRT			X	X							X	X						X					
S_INIT											X												
S_FKG			X								X							X					10 <sub>H</sub> : Input X/XN not S_EA 20 <sub>H</sub> : Input XC/XCN not S_EA 30 <sub>H</sub> : Input YC/YCN not S_EA 40 <sub>H</sub> : ERR divers. comparison 50 <sub>H</sub> : #n too high 60 <sub>H</sub> : ERR writing memory 70 <sub>H</sub> : ERR writing output 80 <sub>H</sub> : ERR result comparison

CE Name	FK2: 510	FK2: 511	FK2: 515	FK2: 516	FK2: 520	FK2: 521	FK2: 522	FK2: 525	FK2: 526	FK2: 527	FK2: 530	FK2: 540	FK2: 541	FK2: 542	FK2: 543	FK2: 544	FK2: 545	FK2: 546	FK2: 547	FK2: 548	FK2: 549	Additional information	Direct ERR output	
<b>Group 3</b>																								
S_=?		X	X								X													
S_<		X	X								X													
S_<=		X	X								X													
S_>		X	X								X													
S_>=		X	X								X													
S_<>		X	X								X													

CE Name	FK2: 510	FK2: 511	FK2: 515	FK2: 516	FK2: 520	FK2: 521	FK2: 522	FK2: 525	FK2: 526	FK2: 527	FK2: 530	FK2: 540	FK2: 541	FK2: 542	FK2: 543	FK2: 544	FK2: 545	FK2: 546	FK2: 547	FK2: 548	FK2: 549	Additional information	Direct ERR output	
<b>Group 4</b>																								
S_&	X	X									X													
S_&N	X	X									X													
S_/	X	X									X													
S_/N	X	X									X													
S_!	X																							
S_IN	X																							
S_=		X																						
S_=N		X																						
S_=S	X	X									X													
S_=R	X	X									X													
S_W/S								X			X													
S_B/S		X			X						X													
S_S/W			X								X													
S_S/B	X					X					X													
S_INSK											X													
S_ISK		X	X								X													
S_=SK	X		X								X													
S_AWTB	X	X									X													

CE Name	FK2: 510	FK2: 511	FK2: 515	FK2: 516	FK2: 520	FK2: 521	FK2: 522	FK2: 525	FK2: 526	FK2: 527	FK2: 530	FK2: 540	FK2: 541	FK2: 542	FK2: 543	FK2: 544	FK2: 545	FK2: 546	FK2: 547	FK2: 548	FK2: 549	Additional information	Direct ERR output
<b>Group 5</b>																							
S_ABO	X										X			X									
S_SPBM	X																						
S_CRC8								X			X												
S_TSYN																			X	X	X		

CE Name	FK2: 510	FK2: 511	FK2: 515	FK2: 516	FK2: 520	FK2: 521	FK2: 522	FK2: 525	FK2: 526	FK2: 527	FK2: 530	FK2: 540	FK2: 541	FK2: 542	FK2: 543	FK2: 544	FK2: 545	FK2: 546	FK2: 547	FK2: 548	FK2: 549	Additional information	Direct ERR output	
<b>Group 6</b>																								
S_ESV	X	X	X								X		X										10 <sub>H</sub> : Input T-0 not S_EB 20 <sub>H</sub> : HM_ESV (from history values memory) not S_EB 30 <sub>H</sub> : Error in comparison T_LOW with -(NT_LOW) 40 <sub>H</sub> : Error in comparison T_HIGH with -(NT_HIGH) 50 <sub>H</sub> : No free timer  60 <sub>H</sub> : ERR write output 70 <sub>H</sub> : ERR Z flag 80 <sub>H</sub> : ERR writing ASAS memory 90 <sub>H</sub> : ERR writing VWS memory 100 <sub>H</sub> : ERR 2. time base	
S_ASV	X	X	X								X		X										10 <sub>H</sub> : Input T-0 not S_EB 20 <sub>H</sub> : HM_ASV (from history values memory) not S_EB 30 <sub>H</sub> : Error in comparison T_LOW with -(NT_LOW) 40 <sub>H</sub> : Error in comparison T_HIGH with -(NT_HIGH) 50 <sub>H</sub> : No free timer  60 <sub>H</sub> : ERR write output 70 <sub>H</sub> : ERR Z flag 80 <sub>H</sub> : ERR writing ASAS memory 90 <sub>H</sub> : ERR writing VWS memory 100 <sub>H</sub> : ERR 2. time base	
S_I+	X	X									X													
S_I-	X	X									X													





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